METHODS OF TESTING INTERCONNECT LINES IN PROGRAMMABLE LOGIC DEVICES USING PARTIAL RECONFIGURATION

ABSTRACT

Methods and systems for testing PLD interconnect lines, e.g., interconnect lines driven by a plurality of programmable buffers. Each programmable buffer has an associated memory element. The memory elements are configured to form a shift register, with one of the buffers and the interconnect line inserted between two of the memory elements. The signal path through the shift register is tested using a first test pattern. Partial reconfiguration is then used to change the insertion point of the interconnect line in the signal path by changing the configuration of the interconnect structure and using a second one of the buffers. A second test pattern is then used to test the second buffer. This sequence is repeated until each of the buffers has been tested. Because only small changes are required, the partial reconfiguration requires loading only small amounts of configuration data, significantly reducing test time compared to presently-known test methods.